Ordering number: EN3680C

Monolithic Linear IC

LA4485

5 W, Two-channel Power Amplifier with Very Few External Parts

Overview

The LA4485 is a 5 W, two-channel power amplifier IC that requires a minimum of external parts, making it ideal for radio cassette players and car stereo equipment.

The LA4485 eliminates the need for bootstrap capacitors, negative feedback capacitors, and oscillation prevention CR parts, all of which were necessities for power ICs previously. All of these functions are now on chip, keeping the number of external parts to an absolute minimum. The LA4485 is part of the Power (Stylish Power) Series, and supports two modes: dual and BTL.

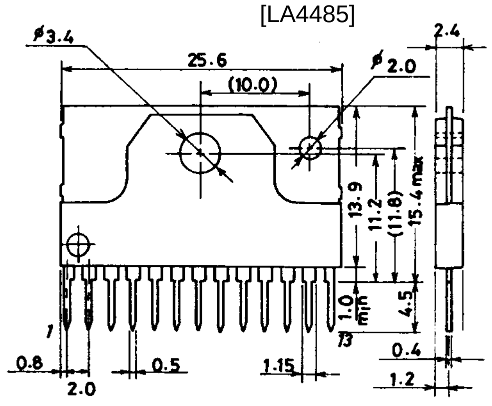
Features

- 5 W × 2 output power in dual mode, and 15 W in BTL mode
- Minimum external parts for the Power Series count: 4 or 5 parts in dual mode; 3 or 4 parts in BTL mode
- Protection circuits
  - Overvoltage protection
  - Thermal protection
  - DC output short-circuit protection (to V_{CC} and to GND)
- Circuitry designed to handle $+V_{CC}$ applied to the outputs
- Pop noise reduction
- Standby switch
- Muting function

Package Dimensions

unit : mm

3107-SIP13H



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	No signal	24	V
Surge supply voltage	V_{CC} surge *	Based on the JASO standard	50	V
Peak output current	I_O peak	Per channel	3.3	A
Allowable power dissipation	Pd max	With infinite heat sink	15	W
Operating temperature	Topr		–30 to +80	°C
Storage temperature	Tstg		–40 to +150	°C

*: By the π type B check point method.

Operating Conditions at Ta = 25°C

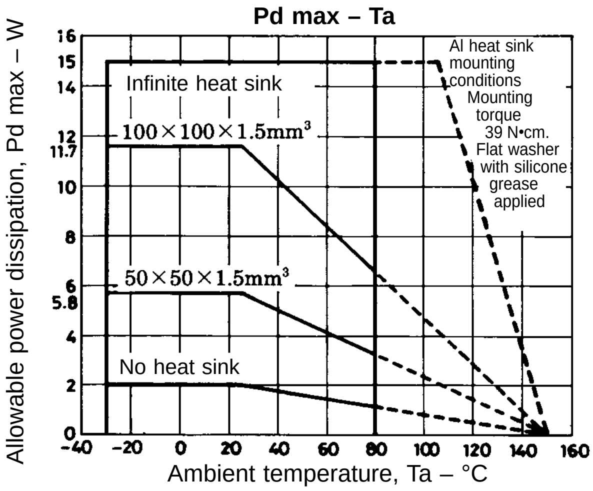
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		13.2	V
Supply voltage range	V_{CC} op	Must not be over package Pd	7.5 to 18	V
Recommended load resistance range	R_L	Dual	2 to 8	Ω
		BTL	4 to 8	Ω

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

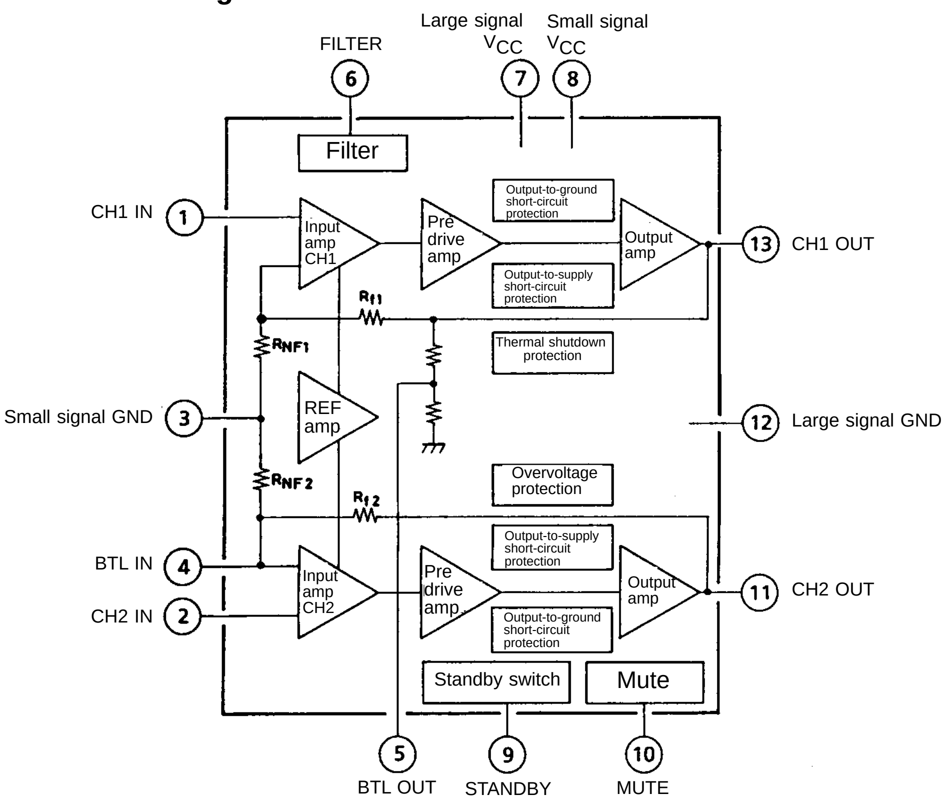
Operating Characteristics at Ta = 25°C, V_{CC} = 13.2 V, R_L = 4 Ω, Rg = 600 Ω, f = 1 kHz, Dual

Parameter	Symbol	Conditions	min	typ	max	Unit
Standby current	Ist	Pin 9 to GND, Standby switch OFF			10	µA
Quiescent supply current	I_{CCO}	Rg = 0	40	80	160	mA
Voltage gain	VG1	Dual: V_O = 0 dBm	43	45	47	dB
	VG2	BTL: V_O = 0 dBm		51		dB
Output power	P_O1*	Dual: THD = 10%	4	5		W
	P_O2	BTL: THD = 10%	11	15		W
Total harmonic distortion	THD	P_O = 1 W		0.15	0.8	%
Channel separation	CH sep	V_O = 0 dBm, Rg = 0	45	55		dB
Output noise voltage	V_{NO}	Rg = 0, 20 Hz to 20 kHz bandpass filter		0.15	0.5	mV
Ripple rejection ratio	SVRR	Rg = 0, 20 Hz to 20 kHz bandpass filter, f_R = 100 Hz, V_R = 0 dBm, decoupling capacitor connected	40	50		dB

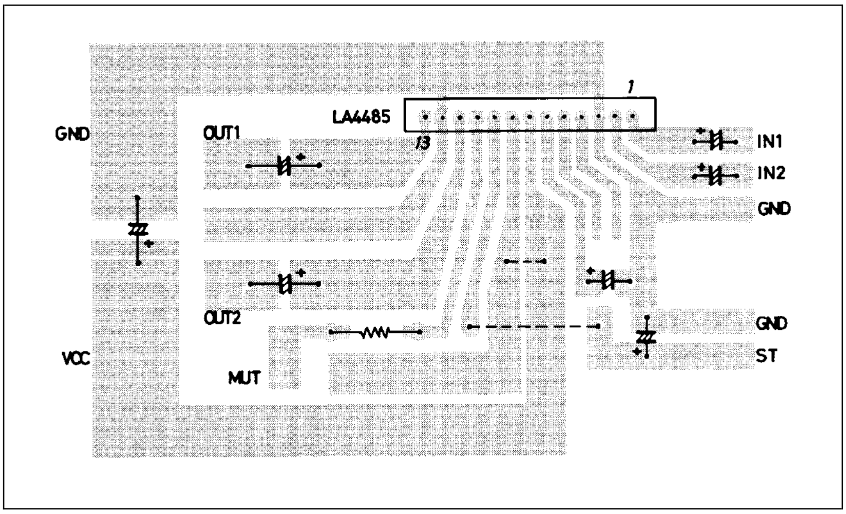
*: P_O1 = 6 W (typ) when V_{CC} = 14.4 V
Voff ± 250 mV for BTL-mode



Equivalent Circuit Block Diagram



Recommended LA4485 External Parts Arrangement (Dual-mode)



95.0 × 67.0 mm^2

IC Usage Notes

Maximum ratings

Care must be taken when operating the LA4485 close to the maximum ratings as small changes in the operating conditions can cause the maximum ratings to be exceeded, thereby breakdown will be caused.

Printed circuit board connections

Care must be taken when designing the circuit of printed board so as not to form feedback loops, particularly with the small-signal and large-signal ground connections.

Notes on LA4485 heatsink mounting

1. Mounting torque must be in the range 39 to 59 N•cm.
2. The spacing of the tapped holes in the heatsink must match the spacing of the holes in the IC tab.
3. Use screws with heads equivalent to truss head machine screws and binding head machine screws stipulated by JIS for the mounting screws. Furthermore, washers must be used to protect the surface of the IC tab.
4. Make sure that there is no foreign matter, such as cutting debris, between the IC tab and the heatsink. If a heat conducting compound is applied between the contact surfaces, make sure that it is spread uniformly over the entire surface.
5. Because the heatsink mounting tab and the heatsink are at the same electric potential as the chip's GND (large signal GND), care must be taken when mounting the heatsink on more than one device.
6. The heatsink must be mounted before soldering the pins to the PCB.

Comparison of External Parts Required

External parts	Existing device	LA4485
Output coupling capacitors	Yes	Yes
Input coupling capacitors	Yes	Yes
Bootstrap capacitors	Yes	No
Feedback capacitors	Yes	No
Filter capacitor	Yes	Optional
Phase compensating capacitor	Yes	No
Oscillation-quenching mylar capacitors	Yes	No
Oscillation-quenching resistors	Yes	No
Others	No	Optional
Total (for dual-mode)	15 to 16 parts	4 to 6 parts

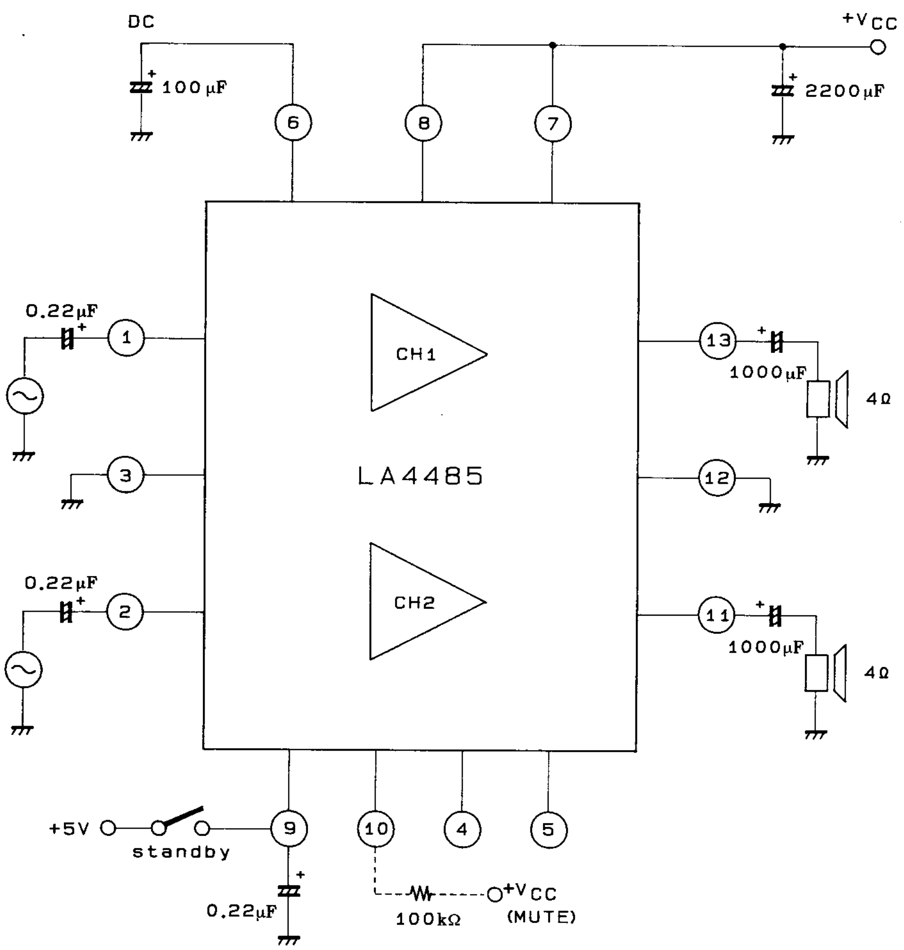
Note: Supply capacitors, contained within the power IC, are not counted in both existing and new devices.

Operating Pin Voltages at V_{CC} = 13.2 V

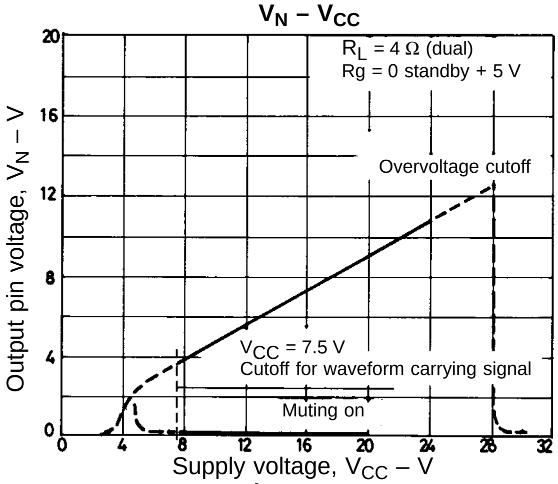
Pin No.	Name	Function	Pin voltage (Reference value)
1	CH1 IN	Channel 1 input.	1.4 V (2 V_{BE})
2	CH2 IN	Channel 2 input.	1.4 V (2 V_{BE})
3	SS GND	Small-signal ground	0 V
4	BTL IN	BTL-mode feedback input.	45 mV
5	BTL OUT	BTL-mode feedback output.	3.1 V (≒1/4 V_{CC})
6	FILTER	Filter capacitor connection.	6.6 V (≒1/2 V_{CC})
7	LS V_{CC}	Large-signal supply	13.2 V (V_{CC})
8	SS V_{CC}	Small-signal supply	13.2 V (V_{CC})
9	STANDBY	Standby control input.	5 V
10	MUTE	Mute control input.	0 V
11	CH2 OUT	Channel 2 output.	6.3 V
12	LS GND	Large-signal ground	0 V
13	CH1 OUT	Channel 1 output.	6.3 V

Note: Each pin is so arranged lest the IC should be broken even if inserted reversely.

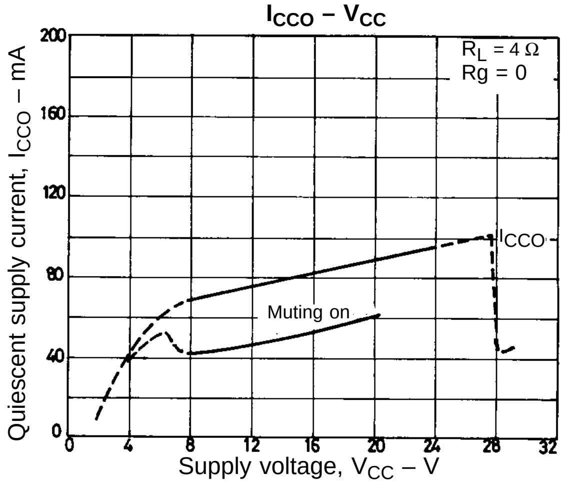
LA4485 Sample Application Circuit



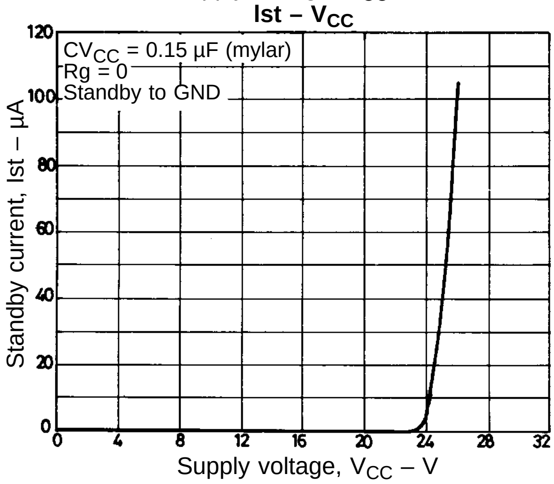
V_N – V_{CC}



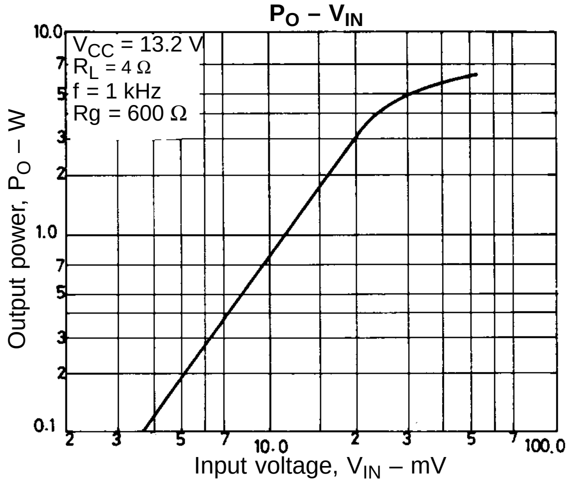
I_{CCO} – V_{CC}



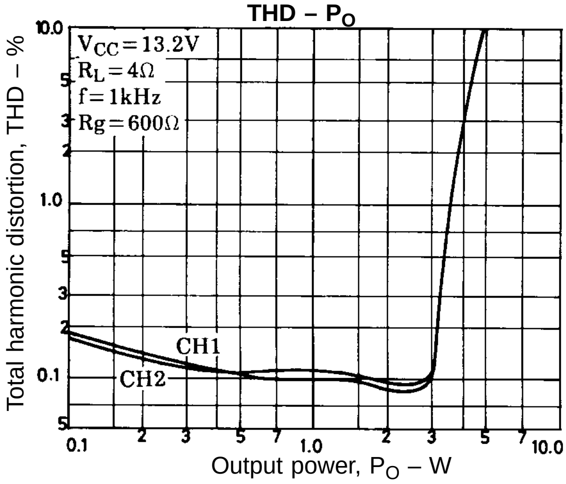
Ist – V_{CC}



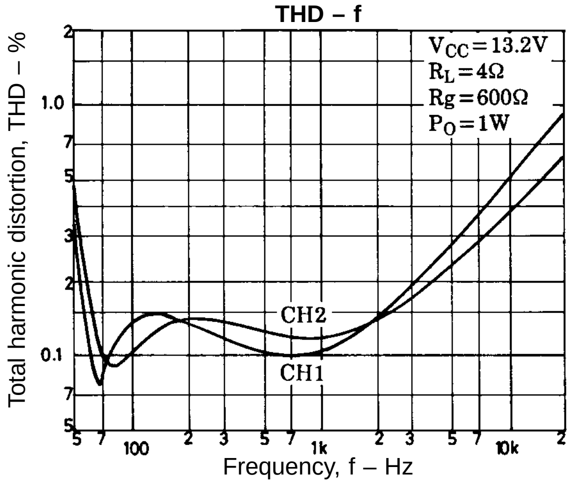
P_O – V_{IN}



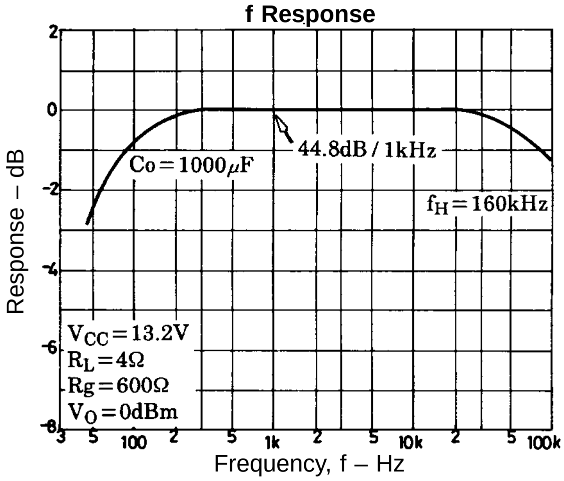
THD – P_O



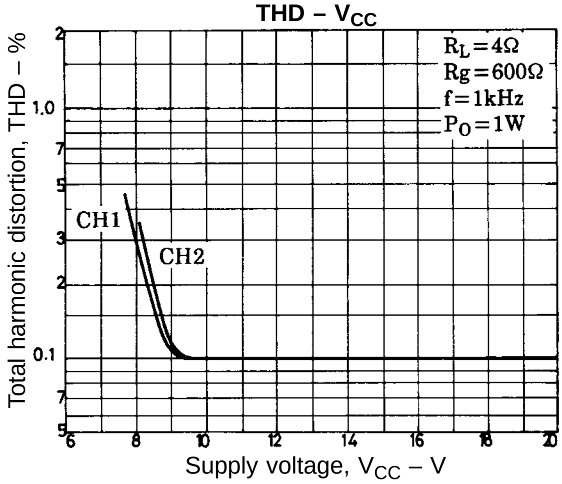
THD – f



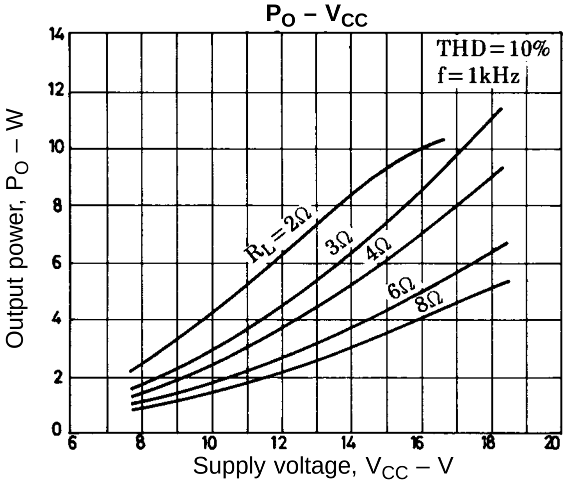
f Response



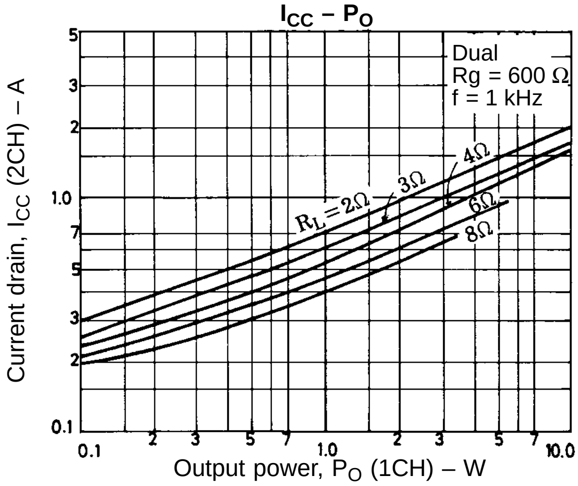
THD – V_{CC}



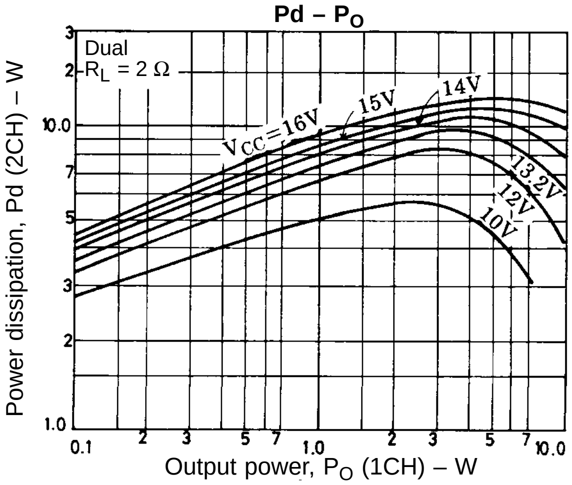
P_O – V_{CC}



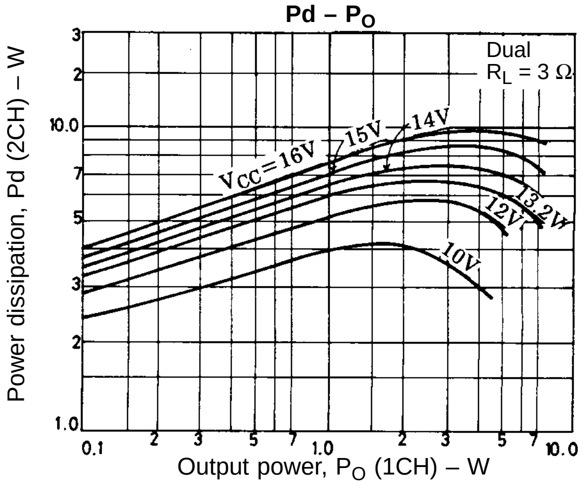
I_{CC} – P_O



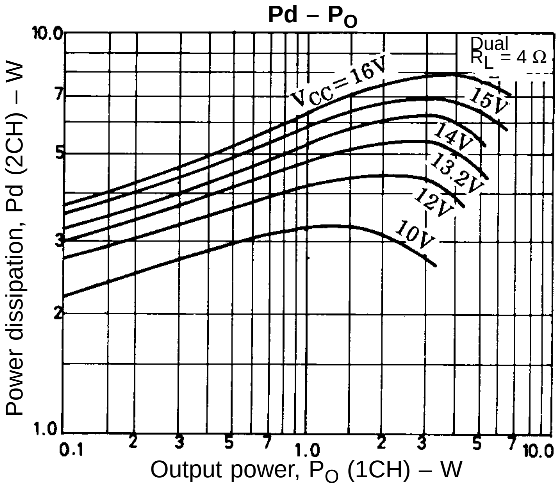
Pd – P_O



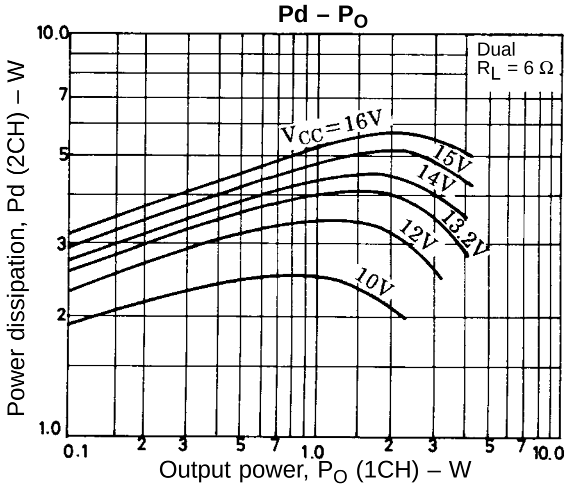
Pd – P_O



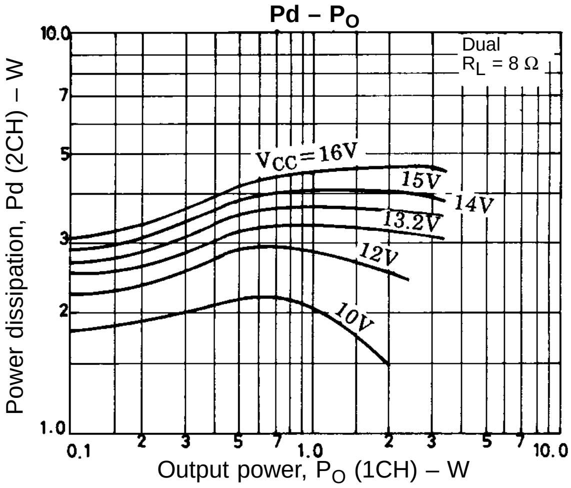
Pd – P_O



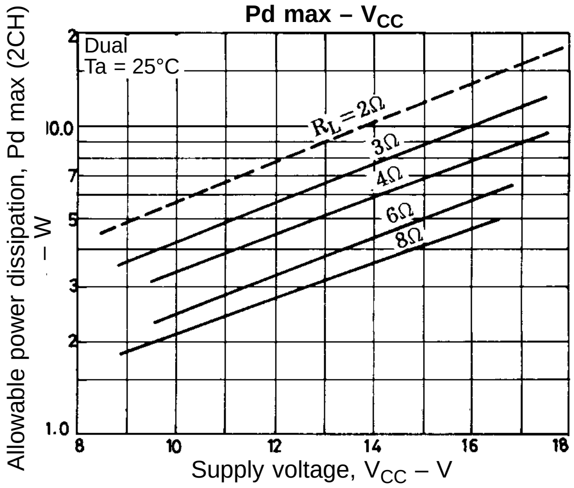
Pd – P_O



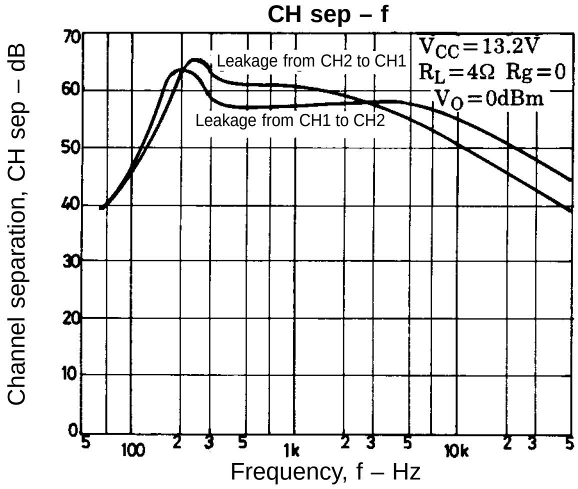
Pd – P_O



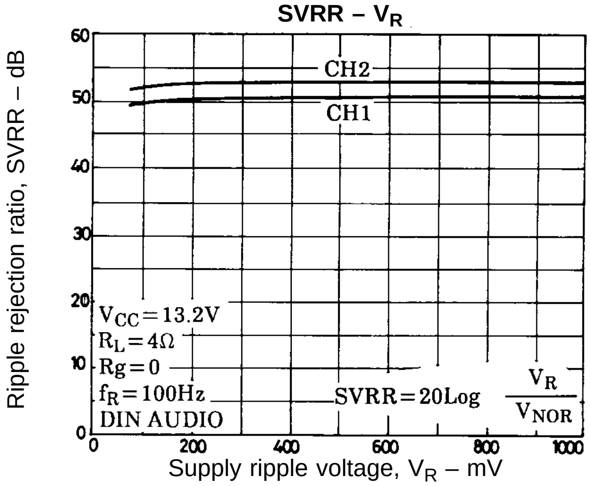
Pd max – V_{CC}



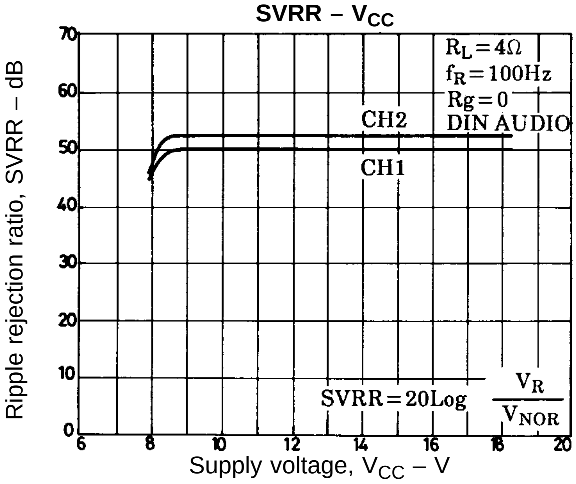
CH sep – f



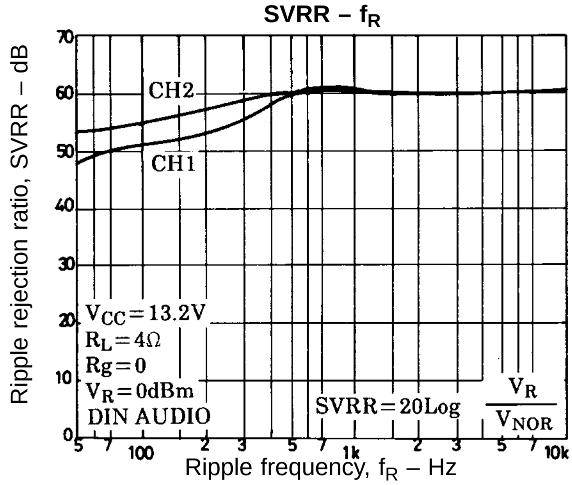
SVRR – V_R



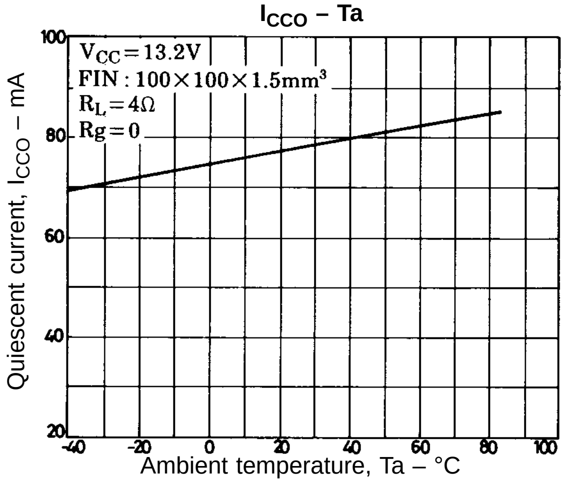
SVRR – V_{CC}



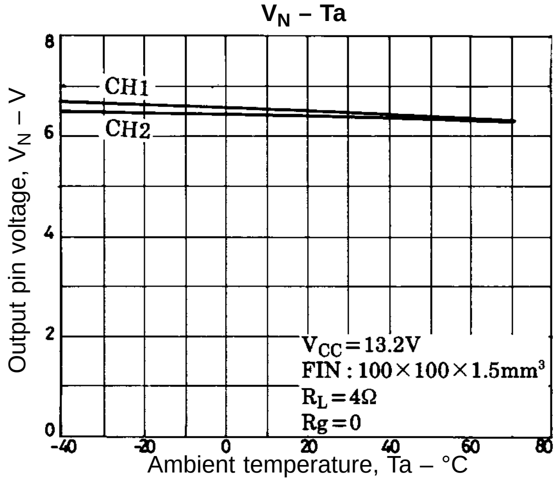
SVRR – f_R



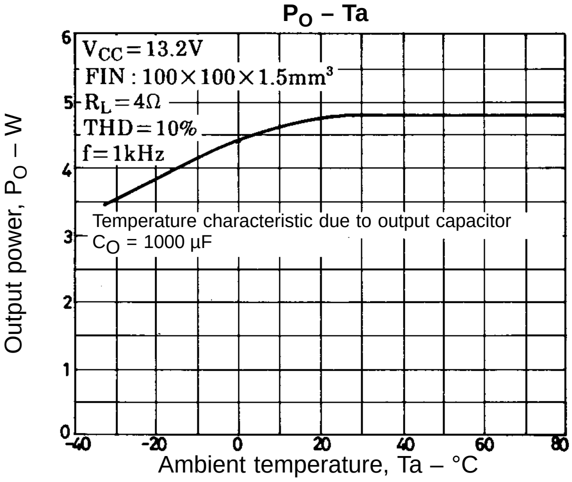
I_{CCO} – Ta



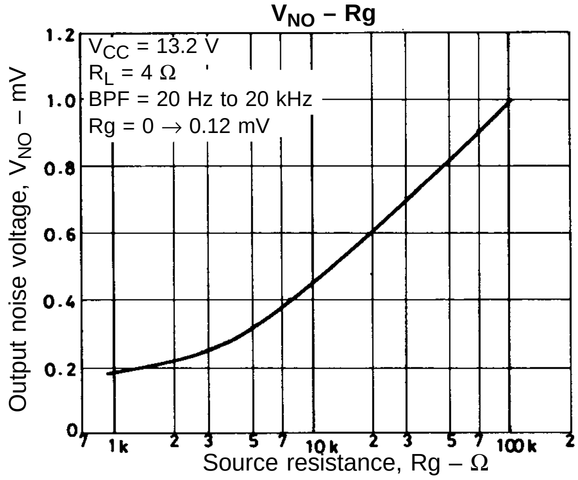
V_N – Ta

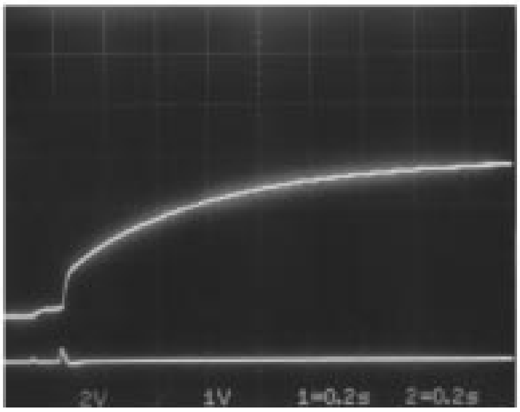


P_O – Ta



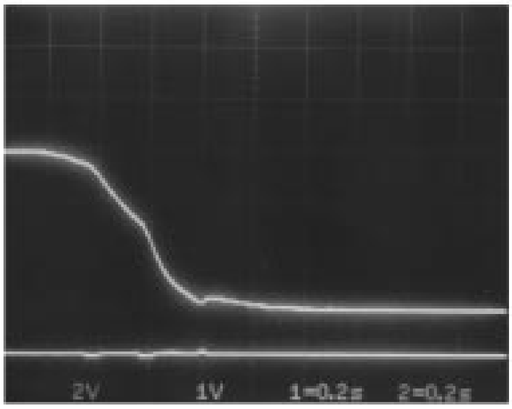
V_{NO} – Rg



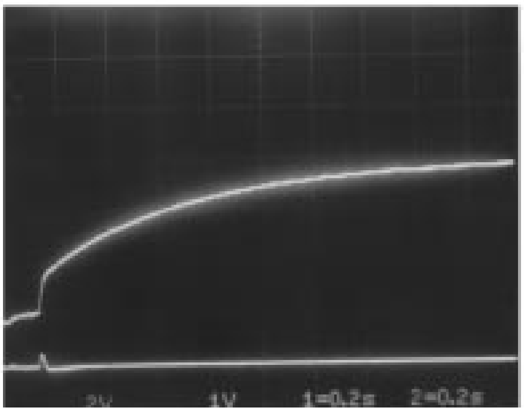


Output
DC trace

Speaker
terminal

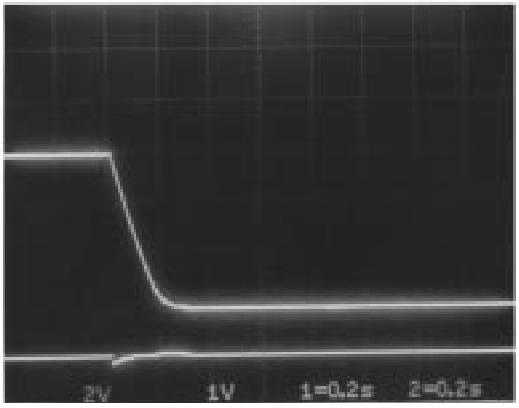


V_{CC} = 13.2 V, standby supply +5 V,
R_L = 4 Ω, Rg = 0
Main switch ON/OFF test

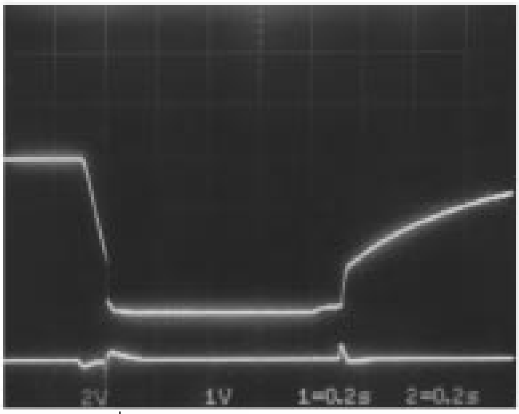


Output
DC trace

Speaker
terminal

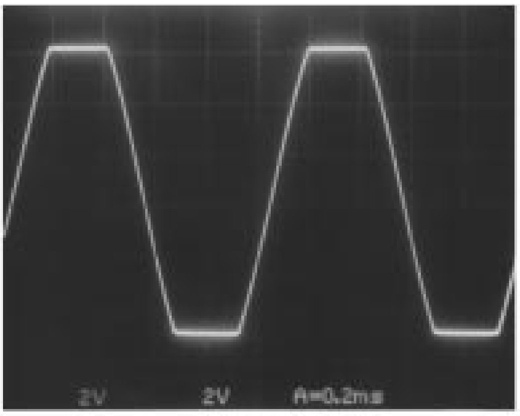


V_{CC} = 13.2 V, standby supply +5 V,
R_L = 4 Ω, Rg = 0
Standby switch ON/OFF text



V_{CC} = 13.2 V,
R_L = 4 Ω,
Rg = 0,
Mute ON/OFF

↳ Switching noise decreases as C_{IN} = 0.22 µF (Input) is increased. (ex. 2.2 µF)



V_{CC} = 13.2 V,
R_L = 4 Ω,
Rg = 600 Ω,
THD = 10%,
f = 1 kHz,
Output DC waveform

Dual-mode Operation Notes

- Use the input capacitor C_{IN} in the range of 0.22 µF to 1.0 µF.

Parameter	C_{IN} = 0.22 µF	C_{IN} = 1.0 µF
Start-up time (ts)	0.15 s	0.25 s
Attack noise when using the muting function	Somewhat noticeable	Good

Speaker turn-ON transient noise increased significantly when C_{IN} is 2.2 µF or greater.

- The DC (filter) capacitor should be 100 µF or greater.

Parameter	100 µF or less	100 µF or more
Standby-off output capacitor discharge circuit	*1. Does not operate. Repeated on/off: poor	*2. Operates normally. On/off: good
Ripple rejection ratio (SVRR)	Somewhat worse 40 dB	Good 50 dB
V_N rise rate when main or standby is turned "on"	Fast	Slow

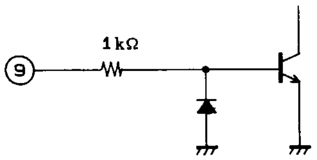
Note:
*1. Slow as a result of natural discharge.
*2. Approximately 0.3 seconds as a result of forced discharge.

- Use the standby supply capacitor in the range of 0.22 µF to 0.47 µF.
  The V_N trace for standby OFF changes and speaker turn-ON transient noise is increased significantly when the capacitor is 1 µF or greater. If the standby function is not used, this capacitor must be removed and pin 9 must be pulled up to the power supply.

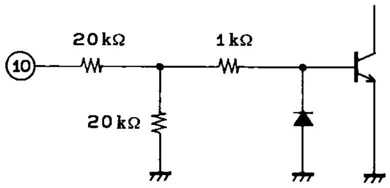
- The output capacitor's recommended value for C_O is 1,000 µF.
  Smaller capacitance will worsen the roll-off frequency f_L and P_O in a low range.

- The recommended power supply capacitor is approximately 2,200 µF, but other capacitors than 2,200 µF can be used according to the application's design.
  Using a capacitor with this value, the load on the supply can be as high as 56 Ω while still providing good supply stability during momentary supply glitches. Note that using a 0.15 µF capacitor can cause oscillations if the supply impedance increases. (Example: Mild oscillation results if the power supply capacitor is open.)

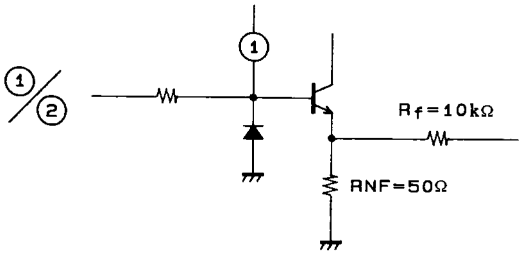
- STANDBY pin 9 IC internal circuit



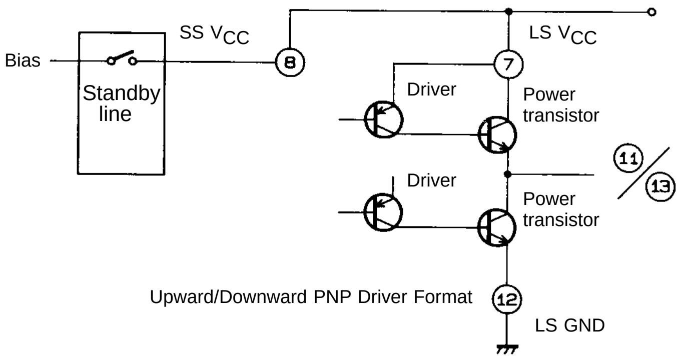
- MUTE pin 10 IC internal circuit



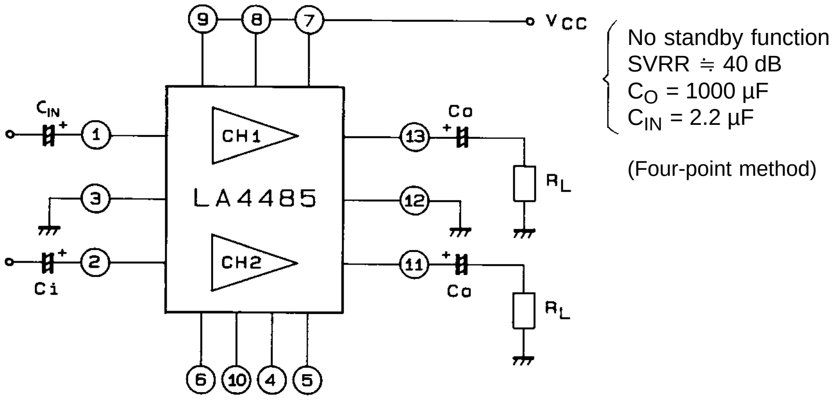
- Input pin 1/2 IC internal circuit



- Output pin 11/13 IC internal circuit

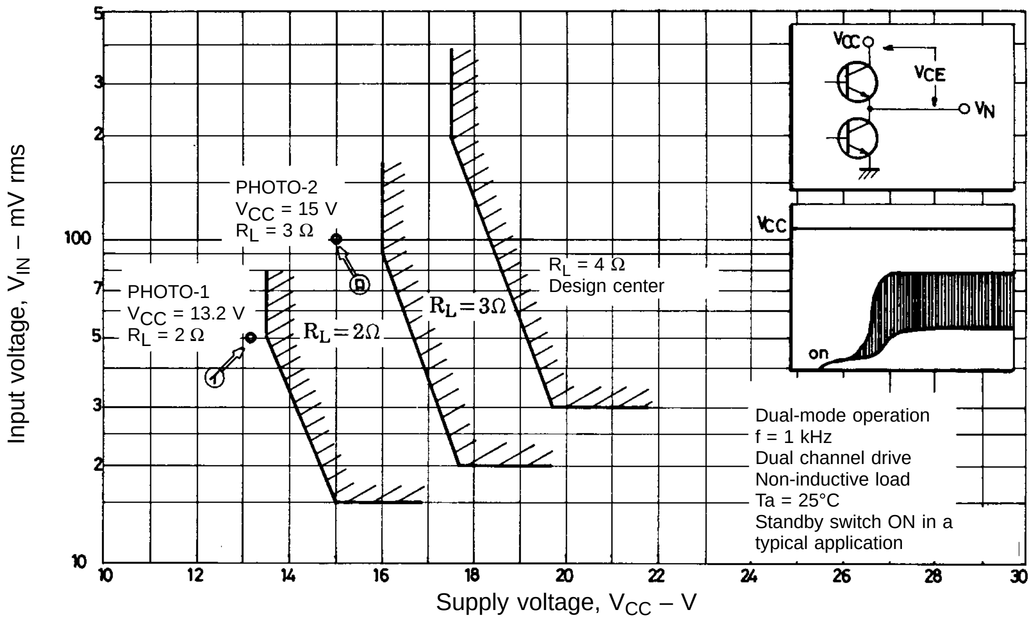


- The minimum configuration for dual-mode operation



- Insert capacitors of 1000 pF between each input and ground to prevent external noise.
- When the load (R_L) or the supply voltage (V_{CC}) is increased, turning the standby switch or the main switch on under strong input conditions will activate the IC's internal pseudo ASO protection circuit for the upper power transistor ($V_{CE} \times I_{CP}$). This causes output oscillations or intermittent operation (The reference area is shown in Figure 1 below). However, strong input tests after the bias has stabilized have no problems. They also protect the upper power transistors close to the limits of ASO when all signal switches are on. Therefore, when using this IC under these conditions, the circuit design should obey the following condition:
  Signal generation time > Start-up time of the power amplifier IC
  or some other method of attaining the zero-volume condition should be adopted.
- An undervoltage protection circuit operates when the voltage is 7.5 V or lower.

This figure shows the pseudo ASO protection area when strong signal is input, and switch is ON: the upper power transistors have an area where $V_{CE} \times I_{CP}$ load is caused.



Strong signal input after switch-ON is OK.
In BTL-mode operation, the load is $R_L \times 2$

Figure 1

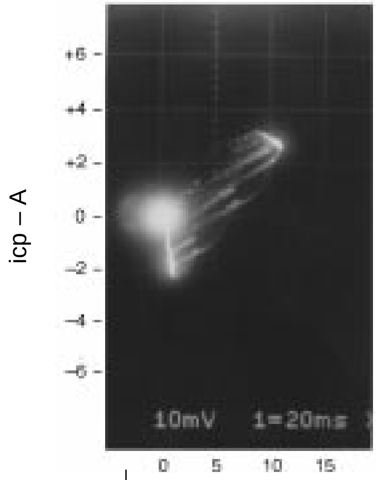
i) The operating condiations for the PHOTO-1 series in dual mode are V_{CC} = 13.2 V, R_L = 2 Ω, f = 1 kHz, V_{IN} = 50 mV and standby switch ON.

"X-Y path observed within the normal area": checking each channel

Output waveforms

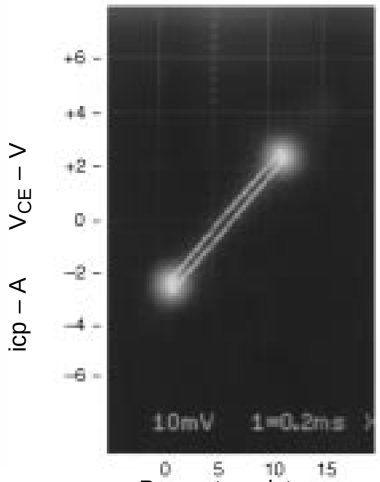


Transition



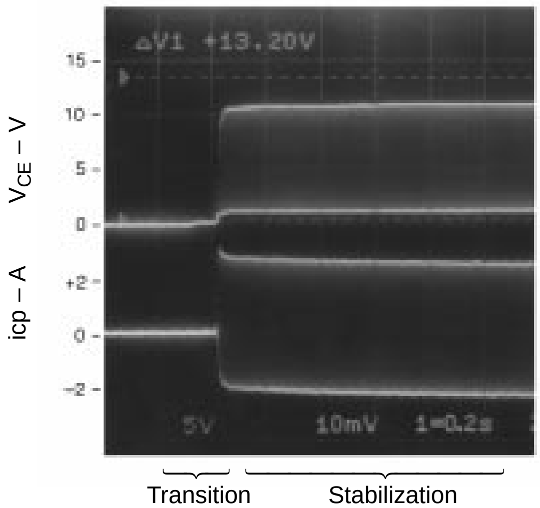
Power transistor CE voltage – V

Stabilization

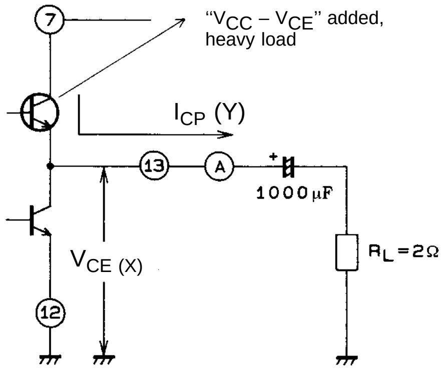


Power transistor CE voltage – V

Current and voltage waveforms



* Plot each point on the power transistor ASO curve. Refer to Figure 2.



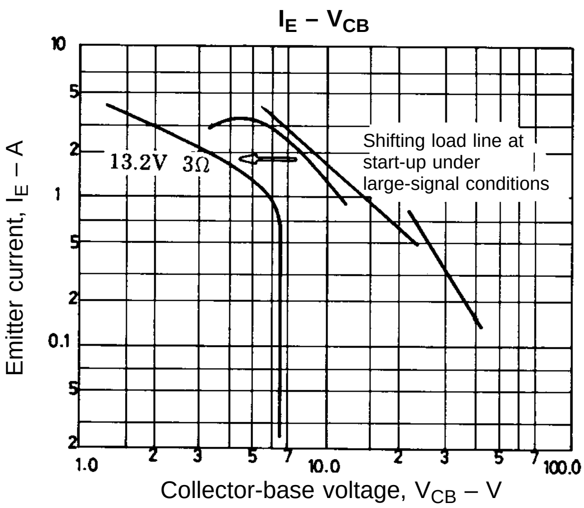


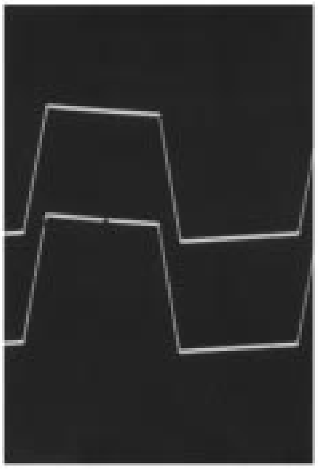
Figure 2

Upper power transistor
The load line becomes more closely aligned with the vertical axis because of the load.

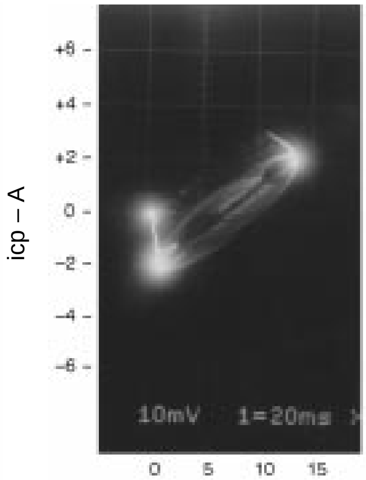
ii) The operating conditions for the PHOTO-2 in dual mode are V_{CC} = 15 V, R_L = 3 Ω, f = 1 kHz, V_{IN} = 100 mV and standby switch ON.

“X-Y path observed within the normal area”

Output waveforms

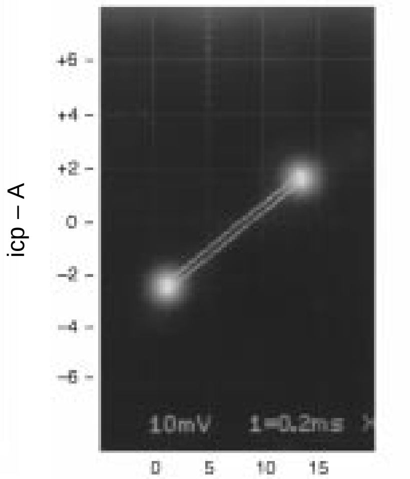


Transition

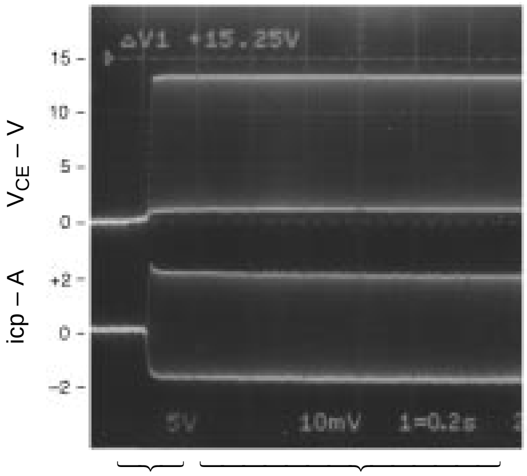


Power transistor CE voltage – V

Stabilization



Current and voltage waveforms



* Plot each point on the power transistor ASO curve. Refer to Figure 3.

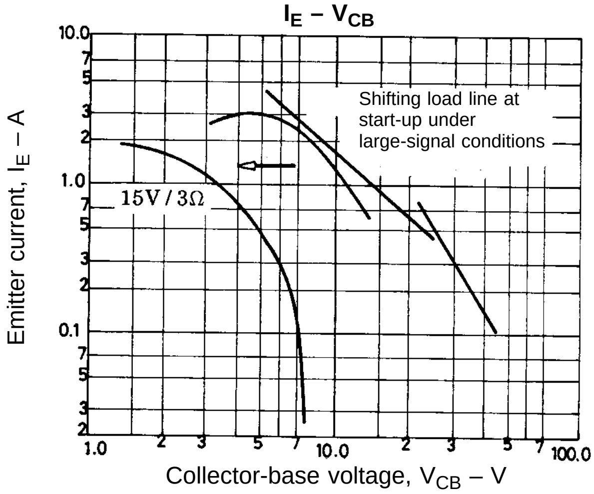
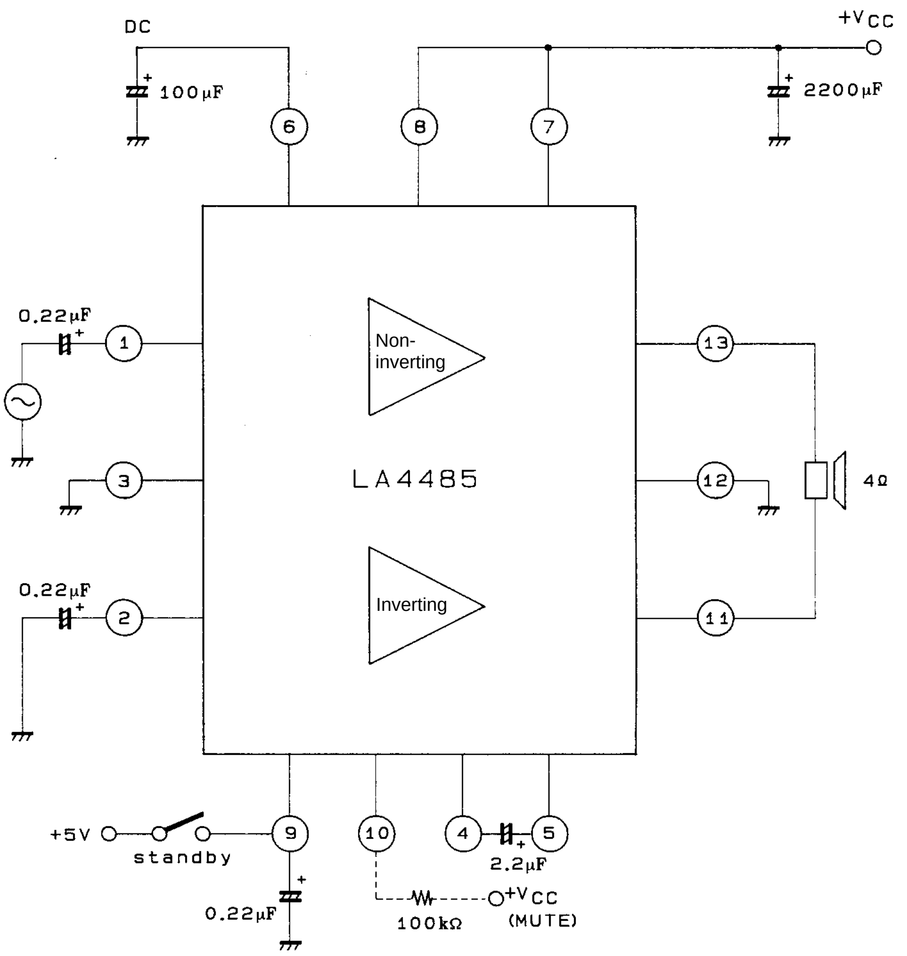
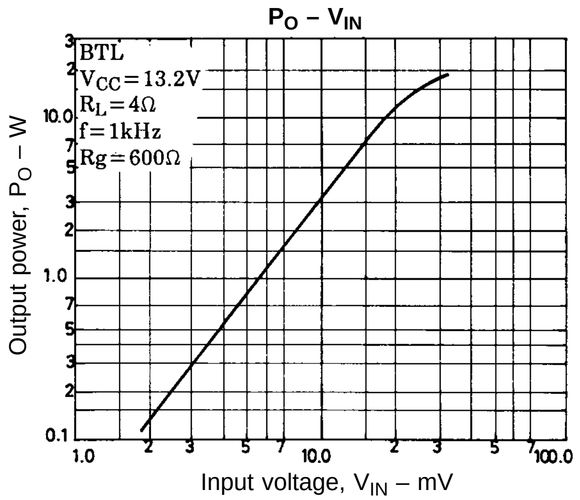
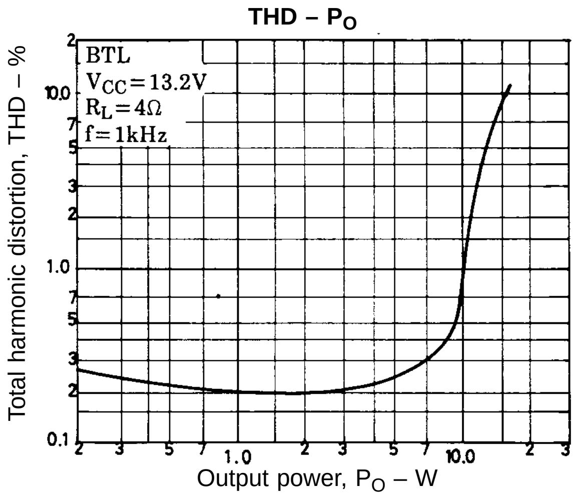


Figure 3

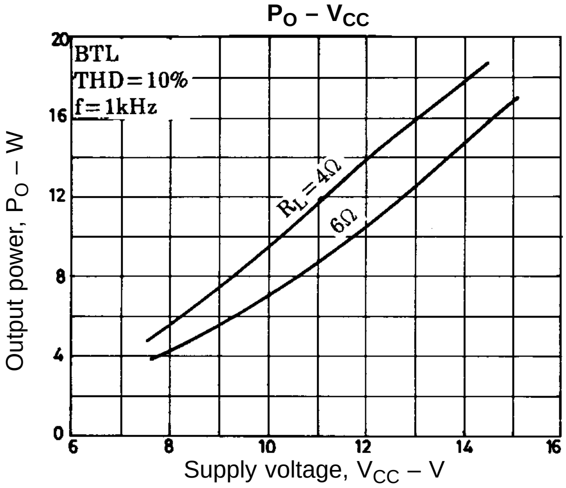
LA4485, BTL Sample Application Circuit



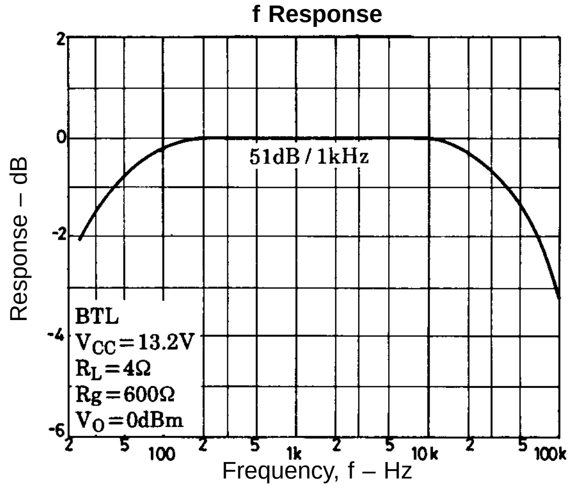




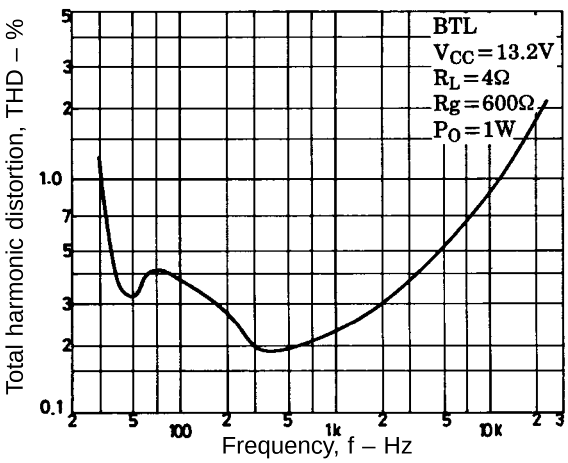
P_O – V_{CC}



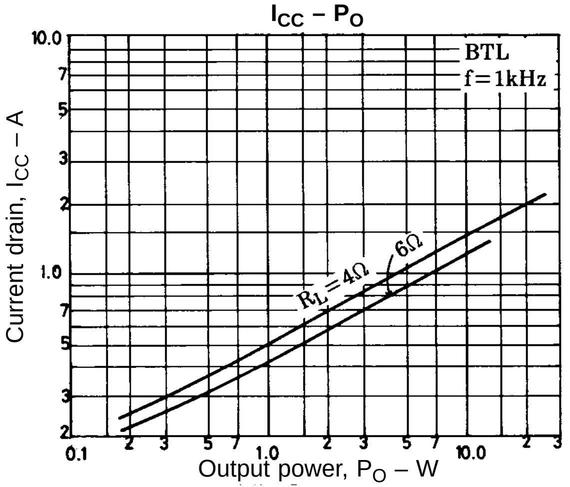
f Response



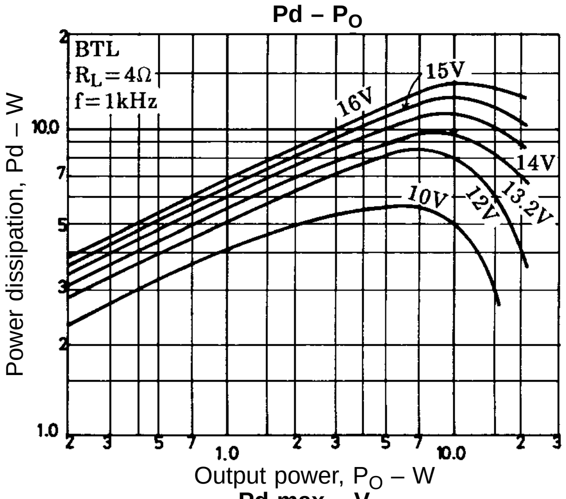
THD – f



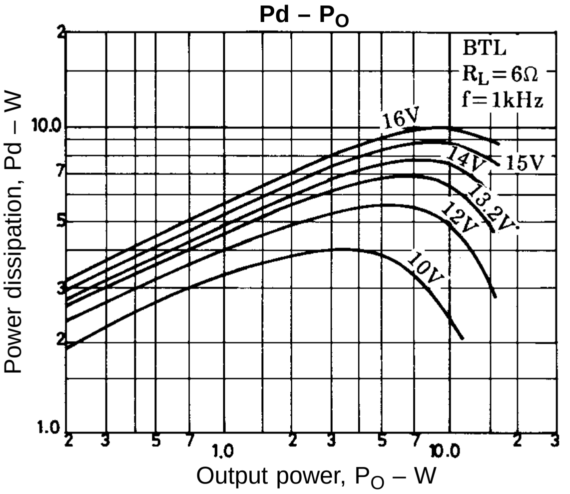
I_{CC} – P_O



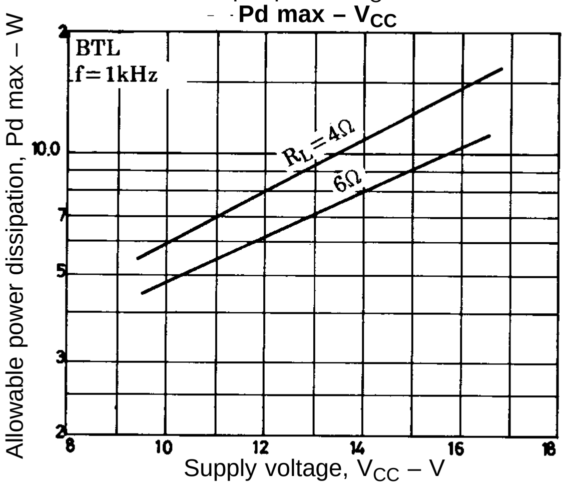
Pd – P_O



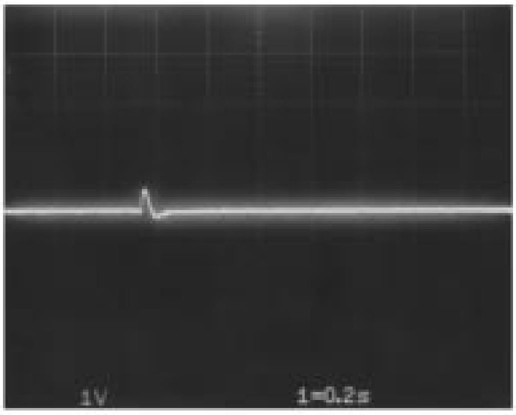
Pd – P_O



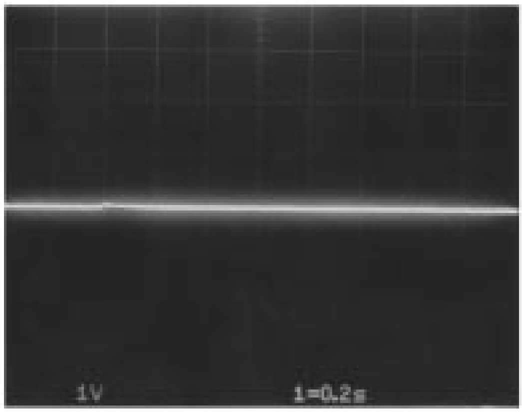
Pd max – V_{CC}



BTL

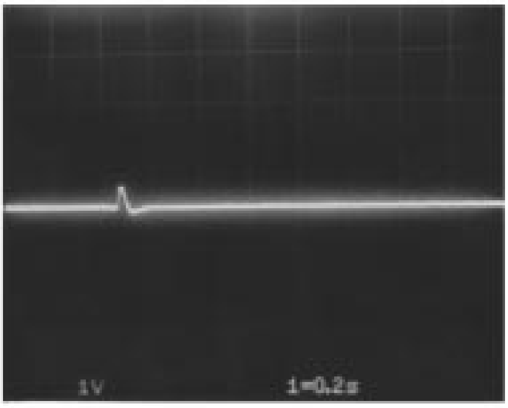


Speaker terminal

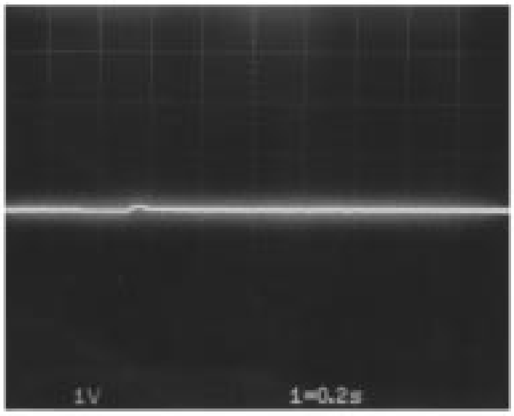


V_{CC} = 13.2 V, standby +5 V,
R_L = 4 Ω, Rg = 0
Main switch ON/OFF test

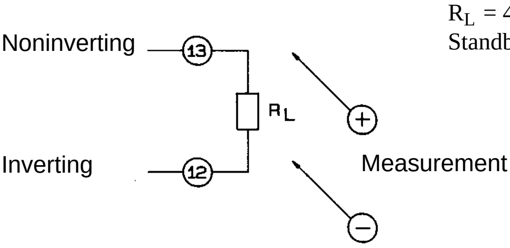
BTL

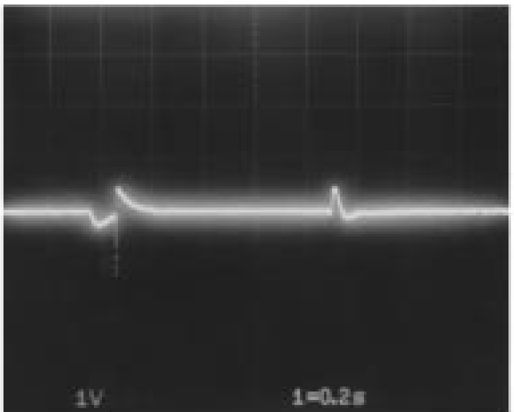


Speaker terminal



V_{CC} = 13.2 V, standby +5 V,
R_L = 4 Ω, Rg = 0
Standby switch ON/OFF test

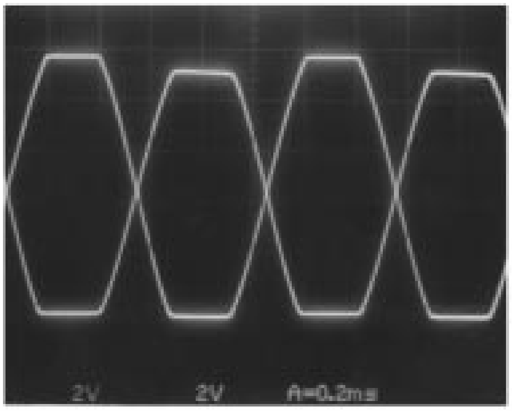




BTL

V_{CC} = 13.2 V
R_L = 4 Ω
Rg = 0
Mute ON/OFF

Note: Switching noise decreases as C_{IN} = 0.22 µF (input) is increased. (ex. 2.2 µF)



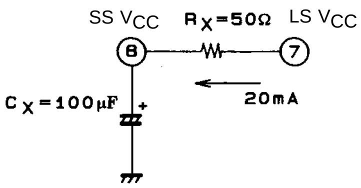
BTL

V_{CC} = 13.2 V,
R_L = 4 Ω,
Rg = 600 Ω,
THD = 10%,
f = 1 kHz
Output DC waveform

BTL-mode Operation Notes

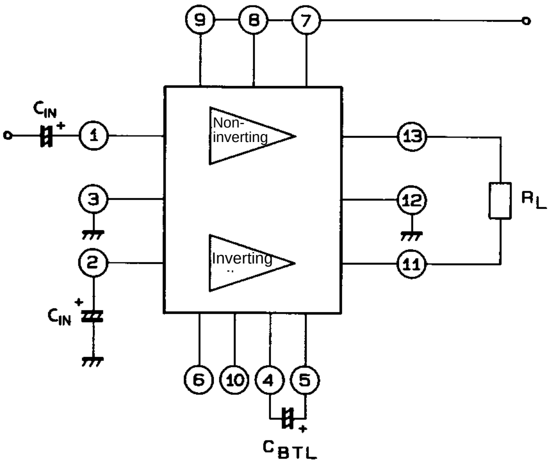
In BTL mode, channel 1 should be non-inverted and channel 2 should be inverted.

- Use the input capacitor C_{IN} in the range 0.22 µF to 2.2 µF.
- Use the standby supply capacitor in the range 0.22 µF to 1.0 µF.
  When the capacitor is 2.2 µF or more, the V_N trace for standby-off changes, and the switching noise increases significantly.
- The recommended DC (filter) capacitor is 100 µF or greater.
- The BTL-mode coupling capacitor should be 2.2 µF.
  When this capacitor is decreased, the output power is decreased. However, when this capacitor is increased, speaker turn-ON transient noise is increased significantly.
- In BTL mode, the ripple rejection ratio (SVRR) is approximately 40 dB.
  This is because the output ripple portion of the noninverted side penetrates the BTL coupling end, so that ripple on the inverted side is large. The following method is described as one external measure:



This measure yields an SVRR of approximately 50 dB. Note that the Rx loss voltage is approximately 1 V, and the P_O loss is about 1.0 to 1.5 W (to the 15 W level).

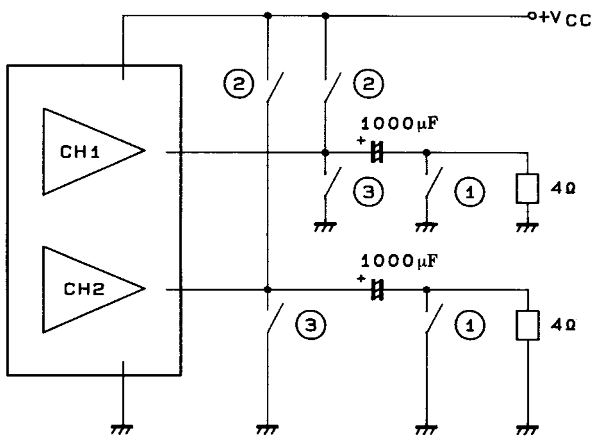
- Example of minimum parts for BTL operation



No standby function
SVRR ≒ 40 dB
C_{IN} = 2.2 µF
C_{BTL} = 2.2 µF

(Three point method)

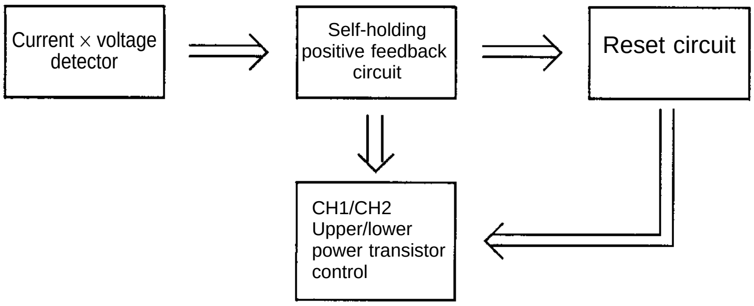
Dual-mode short-circuit test circuit



① Load short-circuit (to ground)
② Output-to-supply short-circuit
③Output-to-ground short-ciruit

- Taking BTL coupling into consideration, the output-to-supply/output-to-ground protector is two-sided in order to protect both the IC and the speaker.

Short-circuit to GND protection



When using this method (simultaneously shorting the outputs to supply and to ground)
In BTL mode, the IC protection function works even in noninverted output → output-to-supply mode, inverted output → output-to-ground mode. (The reverse is also OK.)

Reference Value

(a) Short-circuit test for dual-mode operation after the main and standby switches are turned ON.
Conditions: ① V_{CC} = 10 to 16 V, R_L = 4 Ω and P_O = 1 to 5 W (variable) for load short-circuit
② V_{CC} = 10 to 16 V, R_L = 4 Ω, Rg = 0 (no signal) for output-to-supply short-circuit
③ V_{CC} = 10 to 16 V, R_L = 4 Ω, Rg = 0 (no signal) for output-to-ground short-circuit.

Z: impedance ◯: no device breakdown

① Load short-circuit	② Output-to-supply short-circuit				③ Output-to-ground short-circuit			
	One-time test		Repeated switching test		One-time test		Repeated switching test	
	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω
◯	◯	◯	◯	◯	◯	◯	◯	◯

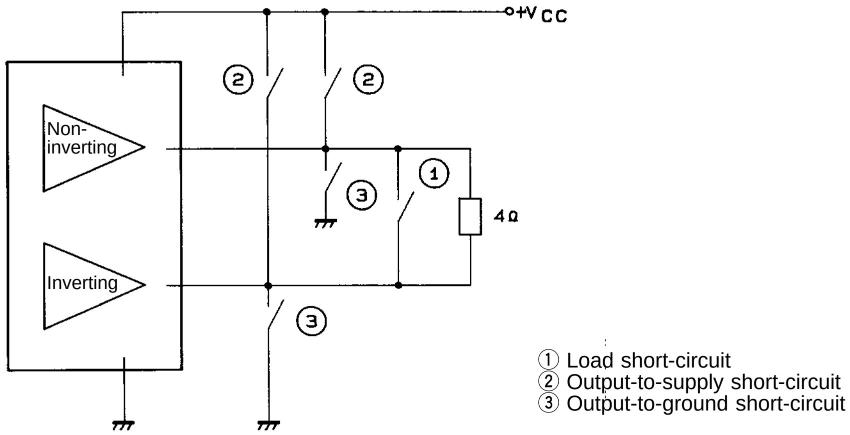
(b) Short-circuit test for dual-mode operation (opposite flow of (a)) after the main and standby switches are turned ON.

Conditions: same as (a) ◯: No device breakdown

① Load short-circuit	② Output-to-supply short-circuit				③ Output-to-ground short-circuit			
	One-time test		Repeated switching test		One-time test		Repeated switching test	
	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω
◯	◯	◯	◯	◯	◯	◯	◯	◯

(Note) Shorting the outputs to ground when muting is active can result in device breakdown.

- BTL-mode short-circuit test circuit



Reference Value

(a) Short-circuit test for BTL-mode operation after the main and standby switches are turned ON.
Conditions: ① V_{CC} = 10 to 16 V, R_L = 4 Ω and P_O = 1 to 15 W (variable) for load short-circuit
② V_{CC} = 10 to 16 V, R_L = 4 Ω, Rg = 0 (no signal) for output-to-supply short-circuit
③ V_{CC} = 10 to 16 V, R_L = 4 Ω, Rg = 0 (no signal) for output-to-ground short-circuit.

Z: impedance ◯: no device breakdown

① Load short-circuit	② Output-to-supply short-circuit				③ Output-to-ground short-circuit			
	One-time test		Repeated switching test		One-time test		Repeated switching test	
	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω
◯	◯	◯	◯	◯	◯	◯	◯	◯

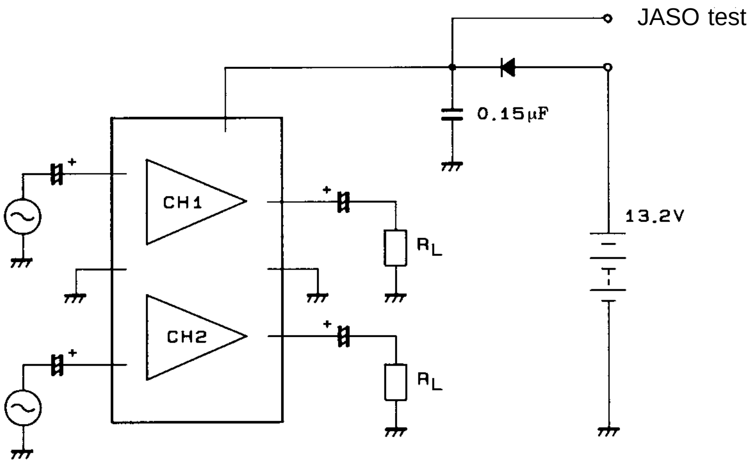
(b) Short-circuit test for BTL-mode operation (opposite flow of (a)) after the main and standby switches are turned ON.

Conditions: same as (a) ◯: No device breakdown

① Load short-circuit	② Output-to-supply short-circuit				③ Output-to-ground short-circuit			
	One-time test		Repeated switching test		One-time test		Repeated switching test	
	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω	Z = 0	Z = 0.5 Ω
◯	◯	◯	◯	◯	◯	◯	◯	◯

(Note) Shorting the outputs to ground when muting is active can result in device breakdown.

- Power supply positive surge



The power supply line positive surge breakdown margin has been increased by using the built-in overvoltage protection circuits (V_{CCX} = 28 V) to cut off all bias circuits/change the base-emitter reverse of the output stage. In other words, the breakdown margin is being raised by changing output stage groups that operate as the V_{CEO} (V_{CER}) type to the V_{CES} (V_{CBO}) type.

• Test of application of $+V_{CC}$ to output pins

If the power supply pin is floating under the power supply capacitor insertion conditions, and $+V_{CC}$ comes into contact with output lines (a) and (b) as shown in the diagram above, the IC’s internal upper power transistor will generally be damaged. The LA4485 has a protective bypass circuit on chip. However, it is dangerous if the power supply capacitor is greater than 2200 µF.

